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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,138	01/25/2002	Edgar R. Zuniga-Ortiz	TI-33986	1847

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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,138	ZUNIGA-ORTIZ ET AL.	
	Examiner	Art Unit	
	Luan Thai	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *3,10-14,16-21 and 24-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-9, 15, 22-23 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/7/04 has been entered.

Claims **1-38** and newly added claim **39** are pending in this application.

Claims ***3, 10-14, 16-21 and 24-38*** have been withdrawn from consideration.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims **1-2, 4-9, 15, 22-23 and 39** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification, as originally filed, does not disclose "*the semiconductor chip having a planar active surface including an integrated circuit protected by an inorganic overcoat with side walls*", and "*a planar outer surface covering the side walls of the inorganic overcoat*", as recited in the amended claim 1.

Claims **2, 4-9, 15, 22-23 and 39** are rejected since each includes the limitations of independent claim **1**.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims **1-2, 4-9, 15, 22-23 and 39** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim **1**, the recitation "*an inorganic overcoat with side walls*" is unclear and not understood as to how to describe the sidewalls of the inorganic overcoat in the applicant claimed structure. Noted that "*with side walls*" is a newly added limitation, which has not been described in the specification. And the examiner assumes that the sidewalls of the inorganic overcoat are the sides of the window of the inorganic overcoat opened over the surface of the contact pad.

Claims **2, 4-9, 15, 22-23 and 39** are rejected since each includes the limitations of independent claim **1**.

Claim Rejections - 35 USC § 102

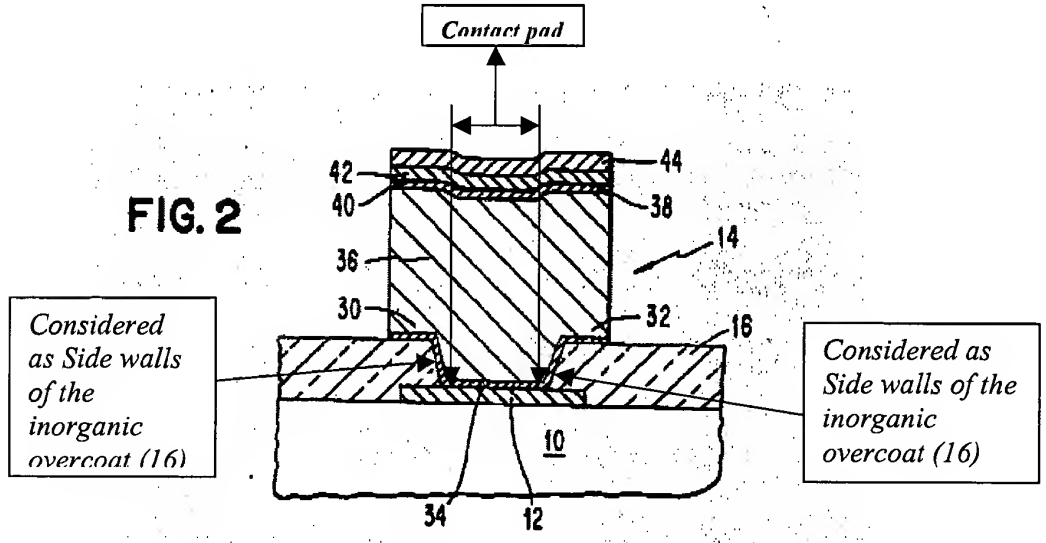
5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 4-9, 15 and 39, insofar as being definite, are rejected under 35 U.S.C. 102(b) as being anticipated by Berndlmaier et al. (5,053,851).

Regarding claims 1, 4-8, 15 and 39, Berndlmaier et al. disclose (see specifically figure **2** attached below) a semiconductor device comprising a semiconductor chip (10) having a planar active surface inherently including an integrated circuit protected by an inorganic overcoat (16) with side walls, the circuit having a plurality of aluminum contact pads (12), each of contact pads (12) having an added conductive layer (34/36/40/42/44) on the metallization (12), the added layer having a conformal surface adjacent the chip, including peripheral portions of the overcoat (16), and a planar outer surface covering the side walls of the inorganic overcoat and defining a flat outline to be substantially parallel to the chip surface, wherein the added conductive layer consists of at least two conductive sub-layers, one being a conductive diffusion barrier (34) of chromium and a bondable layer (44) of gold. Since Berndlmaier et al. disclose that the conductive added layer (44) is made of gold, the outer surface of such gold layer is suitable to form metallurgical bonds without melting.

FIG. 2



Regarding claim 9, Berndlmaier et al. do not explicitly teach that the inorganic overcoat is moisture impermeable and stiff, this feature, however, is taken to be inherent in Berndlmaier et al. device since the inorganic overcoat layer (16) in Berndlmaier et al.'s device is disclosed as "a passivation layer" and it is apparent that a passivation layer has the characteristic of being "moisture impermeable and stiff".

7. Claims 1, 4-9, 15 and 39, insofar as being definite, are rejected under 35 U.S.C. 102(b) as being anticipated by Camilletti et al. (5,693,565).

Regarding claims 1, 4-8, 15 and 39, Camilletti et al. disclose (see specifically figure **4** attached below) a semiconductor device comprising a semiconductor chip (10A) of silicon having a planar active surface (21A) including an integrated circuit protected by an inorganic overcoat (12A) with sidewalls,

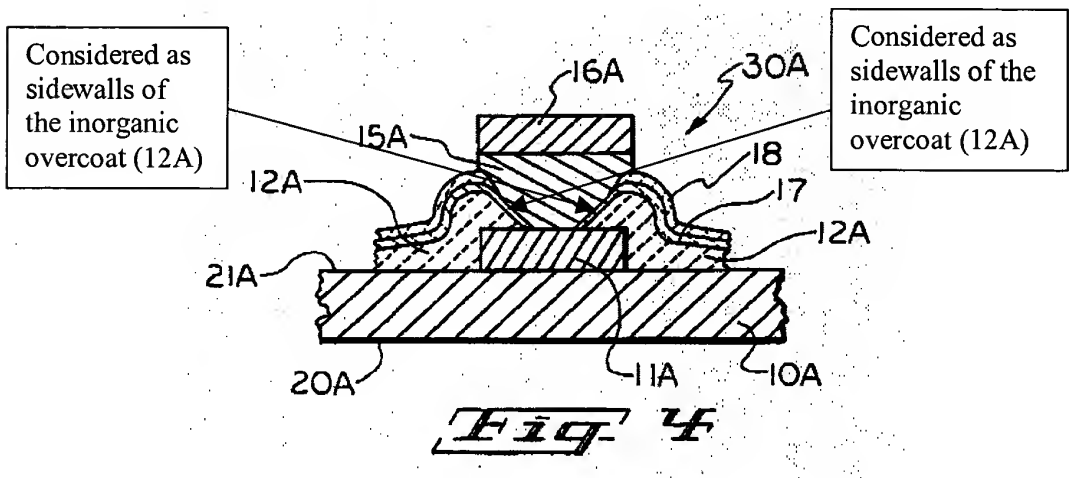


Fig. 4

the circuit having a plurality of aluminum contact pads (11A), each of contact pads having an added conductive layer (15A/16A) on the metallization (e.g., contact pad 11A),

the added layer having a conformal surface adjacent the chip, including peripheral portions of the overcoat (12A), and a planar outer surface covering the side walls of the inorganic overcoat and defining a flat outline to be substantially parallel to the chip surface, wherein the added conductive layer consists of at least two conductive sub-layers (15A/16A), one being a conductive diffusion barrier (15A) of chromium or nickel and a bondable layer (16A) of gold. Since Camilletti et al. disclose that the conductive added layer (16A) is made of gold, the outer surface of such gold layer is suitable to form metallurgical bonds without melting.

Regarding claim 9, Camilletti et al. further teach that the inorganic overcoat is moisture impermeable and stiff (Col. 3, lines46+).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berndlmaier et al. (5,053,851) in view of Fan et al (6,605,524).

Regarding claim 2, Berndlmaier et al. disclose all the limitations of the claimed invention as detailed above except for *a non-conductive layer over the overcoat.*

Fan et al while related to a similar semiconductor package design teach (see specifically figures 13-14) a non-conductive layer (30) of polyimide being over the overcoat layer (14), filling the spaces between the added conductive layers (16/18) on each of the contact pads (12) in order to provide adequate thermal protection to under laying layer (16/18), resulting in a final profile of these layers that does not show bulging and an under-cut, which may occur during the process of making the device (Col. 8, lines 59+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Berndlmaier et al.'s device by applying a non-conductive layer over the overcoat layer and filling the spaces between the added conductive layers on each of the contact pads, as taught by Fan et al., in order to provide adequate thermal protection to under laying layer, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

10. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berndlmaier et al. (5,053,851) in view of Elenius et al (6,287,893 of record).

Regarding claims 22-23, Berndlmaier et al. discloses all the limitations of the claimed invention as detailed above except for another protective layer formed on the chip surface opposite the active surface.

Elenius et al while related to a similar semiconductor structure design teach (see specifically figure 2) a second polyimide layer (34) being formed on the back surface (e.g., the chip surface opposite the active surface) of the semiconductor chip (14) in order to protect the backside of the semiconductor chip. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Berndlmaier et al.'s

device by forming a protective layer on the backside surface of the chip, as taught by Elenius et al, in order to protect the backside of the chip from harmful environmental conditions and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Camilletti et al. (5,693,565) in view of Fan et al (6,605,524).

Regarding claim 2, Camilletti et al. disclose all the limitations of the claimed invention as detailed above except for *a non-conductive layer over the overcoat.*

Fan et al while related to a similar semiconductor package design teach (see specifically figures 13-14) a non-conductive layer (30) of polyimide being over the overcoat layer (14), filling the spaces between the added conductive layers (16/18) on each of the contact pads (12) in order to provide adequate thermal protection to under laying layer (16/18), resulting in a final profile of these layers that does not show bulging and an under-cut, which may occur during the process of making the device (Col. 8, lines 59+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Camilletti et al.'s device by applying a non-conductive layer over the overcoat layer and filling the spaces between the added conductive layers on each of the contact pads, as taught by Fan et al., in order to provide adequate thermal protection to under laying layer, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

12. Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camilletti et al. (5,693,565) in view of Elenius et al (6,287,893 of record).

Regarding claims 22-23, Camilletti et al. discloses all the limitations of the claimed invention as detailed above except for another protective layer formed on the chip surface opposite the active surface.

Elenius et al while related to a similar semiconductor structure design teach (see specifically figure 2) a second polyimide layer (34) being formed on the back surface (e.g., the chip surface opposite the active surface) of the semiconductor chip (14) in order to protect the backside of the semiconductor chip. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Camilletti et al.'s device by forming a protective layer on the backside surface of the chip, as taught by Elenius et al, in order to protect the backside of the chip from harmful environmental conditions and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
Primary Examiner
Art Unit 2829
September 29, 2004